THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte KUO-HUA LEE and JANMYE SUNG

_____

Appeal No. 94-0809
Application 07/707,365[1]

_____

ON BRIEF

_____

Before GRON, PAK and OWENS, Administrative Patent Judges.

GRON, Administrative Patent Judge.

DECISION ON APPEAL UNDER 35 U.S.C. § 134

1. Introduction

This is an appeal from an examiner's rejection of Claims 1-3 and 6, all claims pending in this application. Claims 4 and 5

[1] Application for patent filed May 30, 1991.

were canceled by amendment filed July 16, 1992 (Paper No. 7).

Claims 1-3 and 6 stand finally rejected under 35 U.S.C. § 103 over the teaching of Nishizaka, U.S. 4,981,812, patented January 1, 1991, in view of the combined teachings of Godejahn, U.S. 4,506,437, patented March 26, 1985, and O'Mara et al. (O'Mara), U.S. 5,027,187, patented June 25, 1991, based on an application filed Nov. 6, 1990. Claim 1 reads:

> 1. A method of semiconductor integrated circuit manufacturing comprising the steps of:
>
> forming insulating regions on a substrate;
>
> fabricating gate structures on said substrate between the insulating regions thereby forming regions between said gate structure and said insulating regions, said gate structures having insulating sidewalls, a conducting layer, and an insulating top layer comprising a first material;
>
> making polysilicon plugs between said gate structure and said insulating regions;
>
> implanting impurities into said plugs;
>
> oxidizing the surfaces of said plugs and said first material thereby causing said impurities to diffuse into the substrate to form source/drain regions of a field effect transistor, said gate structure being between said source and said drain regions;
>
> patterning to expose at least selected portions of the gate structure;
>
> etching to remove both the oxide on top of the first material and said first material, thereby exposing portions of said conducting layer but leaving oxide on top of the polysilicon plugs; and

forming an electrical contact to said gate structure, said contact extending over said source/drain regions and extending to said insulating regions.

2. Discussion

When comparing the invention appellants claim to the subject matter the prior art disclosed or would have reasonably suggested to a person having ordinary skill in the art, both the examiner and appellants have in this case overemphasized the semiconductor integrated circuits depicted in Figs. 1-6 of this specification, which were manufactured in accordance with the method appellants claim, and the integrated circuits depicted in Figs. 3(A-L)-5 of Nishizaka. We believe their focus on the differences between the structures of the integrated circuits depicted in appellants' and Nishizaka's figures rather than on the steps of the methods of manufacturing the integrated circuits broadly claimed and described by the cited prior art has brought confusion to this case. We remind both appellants and the examiner that the patentability of the claimed method and its scope and content is the issue on appeal. Just as a product's patentability may not be determined by the patentability of the method by which the product is made, In re Thorpe, 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985) and In re Pilkington, 411 F.2d 1345, 1348,

162 USPQ 145, 147 (CCPA 1969), so the patentability of a novel method of manufacturing a product may not be limited by the patentability of the product made.

For example, appellants argue that Nishizaka forms trenches and fills them with polycrystalline silicon which "may be doped with impurities to be the same conduction type as that of the substrate" (col. 4, l. 16-18) and emphasize that Nishizaka's trenches are not identical in "structure" to the polysilicon[2] plugs depicted in their drawings (Reply Brief (RB.), p. 1, third para.; emphasis added):

> There is a fundamental reason why Nishizaka does not teach or suggest these steps, and this reason is founded in the details of the structure taught by Nishizaka. The polysilicon plugs 10 (i.e., the buried polycrystalline silicon layer) of Nishizaka are not part of or over the source/drain regions of Nishizaka. Nor are they part of the device; rather, the trenches are used to separate elements.

Appellants argue that because of this different "structure" (id.), "Nishizaka refers to the function of these trenches as 'element separating trenches.' Thus, the trenches serve no purpose other than to isolate elements; that is, they do not function as source/drain regions" (Brief on Appeal, p. 3, first

[2] Polysilicon is another name for polycrystalline silicon. See Godejahn, col. 2, l. 7-9 ("A doped polycrystalline silicon layer is applied to such a wafer and a silicon nitride layer is then applied atop the polysilicon layer.")

para.). Some confusion appears to stem from appellants' apparent acknowledgment thereafter that Nishizaka does make polysilicon plugs and may implant impurities into said plugs at least within the meaning of the terms in their claims. Appellants state, "[t]he polysilicon plugs 10 (i.e., the buried polycrystalline silicon layer) of Nishizaka are not part of or over the source/drain regions of Nishizaka" (RB., p. 1, third para.; emphasis added). Had appellants emphasized comparative function rather than comparative "structure," this appeal might not have been necessary.

That the examiner's ultimate decision on the patentability of the claimed subject matter is erroneous in this case is not readily apparent from the respective analyses of Nishizaka's disclosure in the Examiner's Answer (Ans.) and Appellants' Brief on Appeal (Br.). However, because we find that the impurities with which Nishizaka's buried polycrystalline silicon layer 10 may be doped would not "diffuse into the substrate to form source/drain regions of a field effect transistor" (emphasis added), we are constrained to reverse the examiner's holding of unpatentability under 35 U.S.C. § 103 over the combined teachings of Nishizaka, Godejahn, and O'Mara.

The examiner finds (Ans., pp. 4-5, bridging para.):

> Nishizaka teaches a process of forming an integrated circuit substantially as claimed including forming an oxide layer 3 and insulation regions 2 on a substrate 1, depositing a polysilicon layer 4 on said oxide film 3, forming an oxidation film 5 and a silicon nitride layer 6 on said polysilicon layer 4 (Fig. 3(A)), etching said layers 4, 5, and 6 to form gate structure having insulation sidewalls 9, a gate electrode 4, and insulation layers 5 and 6 on top of said gate electrode 4 (Fig. 3(C)), forming polysilicon plugs 10 between gate electrode 4 and insulation region 2 (Fig) 3(E)), doping impurities into said polysilicon plugs 10 (col.4, lines 10-20), oxidizing surface of said polysilicon plugs 10 to form an oxidation layer 11 on top of said plugs 10, connecting a source electrode 16 to said polysilicon plugs 10 (col. 5, lines 1-4 and Fig. 3(L)), etching said oxidation film 5 and said nitride layer 6 to expose a portion of gate electrode 4, and forming an interconnection layer 12 connected to said exposed electrode 4.

Appellants do not contest these findings. Moreover, after examining Nishizaka's disclosure, we cannot conclude with confidence that the examiner's findings are clearly erroneous.

Fig. 3A shows that "a p-semiconductor substrate 1 is selectively oxidized on a predetermined region to provide a field oxidation film 2" (col. 3, l. 53-55), "a gate oxidation film 3 . . . is formed . . ." (col. 3, l. 55-56), "a poly-crystalline silicon layer 4 . . . is grown on the substrate 1 having the gate oxidation film 3 thereon" (col. 3, l. 57-60), "a mask oxidation film 5 . . . is formed on the polycrystalline silicon layer 4" (col. 3, l. 60-62), and "a silicon nitride film 6 is formed on the mask oxidation film 5" (col. 3, l. 63-65).

Fig. 3A does not show a plurality of "insulating regions on a substrate." However, Nishizaka teaches at col. 1, l. 18-24:

> In a conventional process for providing the trench separation, field oxidation films are formed at predetermined regions on a p-semiconductor substrate by use of a selective oxidation method at a first stage. Although plural field oxidation films are provided on plural regions of the substrate, a limited section including only one field oxidation film will be explained hereinafter.

Fig. 3B shows that all the aforementioned films and layers "and an upper portion of the substrate 1 are selectively etched to provide element separating trenches 8" (col. 3, l. 66, to col. 4, l. 2).

Fig. 3C shows that the "inner surface of the element separating trenches 8 is oxidized to provide trench oxidation films 9" (col. 4, l. 3-5).

Fig. 3D shows that "the trench oxidation films 9 are removed on the bottom surface" (col. 4, l. 10-11), "a polycrystalline silicon layer 10 is grown on an overall surface . . . so that the element separating trenches 8 are buried with polycrystalline silicon layer 10" (col. 4, l. 12-16) which "may be doped with impurities to be the same conduction type as that of substrate 1" (col. 4, l. 17-18), and "the polycrystalline silicon layer 10 is etched back on the silicon nitride film 6" (col. 4, l. 18-20).

Figs. 3B-C depict gate structures fabricated when the structure of Fig. 3A is selectively etched to form a repeat of gate structures and separating trenches positioned between insulating regions (not depicted).

Fig. 3D depicts "polysilicon plugs" made by applying polycrystalline silicon over the entire substrate and filling the trenches. Nishizaka's polycrystalline silicon-filled trenches may be implanted or "doped with impurities to be the same conduction type as that of the substrate 1" (Nishizaka, col. 4, l. 16-18).

Figs. 3E-F show that "the polycrystalline silicon layer 10 is etched back . . . by use of the silicon nitride 6 as a mask" for the gate structure (col. 4, l. 21-23) and "insulating oxidation films 11 are formed on the top surface of the polycrystalline silicon layer 10 and on the sides of the polycrystalline silicon layer 4" (col. 4, l. 23-26) and on the silicon nitride 6 used as a mask.

However, we can and do find that Nishizaka's formation of insulating oxidation films 11 on the top surface of the polycrystalline silicon layers 10 and on the silicon nitride 6 mask does not cause the impurities with which polycrystalline silicon layer 10 may be doped "to diffuse into the substrate to form source/drain regions of a field effect transistor." We note

that this finding is entirely consistent with the examiner's finding that Nishizaka "fails to show forming source and drain regions by implanting dopants into silicon plugs and diffusing impurities from the doped polysilicon plugs into the substrate" (Ans., p. 5, first full para.).

Our finding appears also to be consistent with the conventional processes of making the integrated circuits which Nishizaka describes in the BACKGROUND OF THE INVENTION, cols. 1-2. Nishizaka teaches that conventionally (col. 1, l. 31-51; emphasis added):

> . . . a trench oxidation film is formed on the inner surface of the element separating trenches, and an oxidation film is then formed on the silicon nitride film and the trench oxidation films by providing an oxide having a high re-flow property such as BPSG, etc. After this, the high re-flow property oxidation film is re-flowed by a heat treatment of approximately 900^{o} to 1000^{o} C.
>
> At the following stage, the re-flowed oxidation film is etched back to be left in the element separating trenches, so that the top surface of the film is above the top surface of the p-semiconductor substrate, and the silicon nitride film and pad oxidation film are successively removed. Then, a gate oxidation film is formed on the p-semiconductor substrate thus processed, and a polycrystal silicon layer and a WSi layer are successively grown on the gate oxidation film.
>
> Thereafter, a gate electrode is provided by defining the polycrystalline silicon layer and the WSi layer to be a predetermined pattern, and <u>impurities are then injected to provide a source and a drain of a transistor</u> . . . .

Nishizaka teaches that by burying polycrystalline silicon layer 10 in trenches encased by an oxidation film 9, substrate 20 is effectively held at the ground potential in a stable manner (Nishizaka, col. 5, l. 28-33). Nishizaka nowhere suggests that his process causes the impurities with which the polycrystalline silicon layer 10 "may be doped" to diffuse into the substrate to form source/drain regions of a field-effect transistor (Ans., p. 5, first full para.). To the contrary, Nishizaka expressly states (col. 5, l. 44-58):

> Therefore, [the (sic)] following advantages are obtained in the invention.
>
> . . . . .
>
> (2) A short circuit is avoided between digit lines, because no charge is accumulated in a polycrystalline silicon layer which is buried into element separating trenches. Furthermore, if the polycrystalline silicon layer is connected to a semiconductor substrate, and connected through a source electrode to the ground potential, the semiconductor substrate is easily connected to the ground potential, so that the transistor operates with a stable characteristic.

It is difficult for this panel to understand how the polycrystalline silicon layers buried into the separating trenches can "form source/drain regions of a field effect transistor" and impart the advantage of functional stability to Nishizaka's invention when doping the buried polycrystalline silicon layers with impurities is entirely optional.

We have given the language of appellants' claimed process its broadest reasonable interpretation consistent with the description of the invention in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). We have reviewed the examiner's findings with regard to the teachings of the cited prior art. While we cannot agree with appellants' view that the "element separating trenches . . . serve no purpose other than to isolate elements" (Br., p. 3, first para.), we hold that the examiner's rejection is neither supported by objective evidence nor reasonable. We restate here that the examiner has the initial burden to establish a prima facie case of obviousness under 35 U.S.C. § 103. In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Appellants argue that (1) the examiner is reading Nishizaka too broadly and (2) Nishizaka's polysilicon plugs 10, i.e., the buried polycrystalline silicon layers 10, are not part of or over the source/drain regions (RB, p. 1, third para.). Appellants' argument is supported by the greater weight of evidence in this record. However, our deliberations are not therefore put to rest. Appellants' claims stand rejected under 35 U.S.C. § 103 in view of the combined teachings of Nishizaka, Godejahn and O'Mara.

The examiner seems to rely upon the teachings of Godejahn and O'Mara for motivation to form a field effect transistor

having source and drain regions by oxidizing doped polysilicon plugs and/or by implanting dopant impurities into polysilicon plugs and diffusing impurities from polysilicon plugs into a substrate (Ans., p. 5, final two para.). What the examiner has not explained and we do not find apparent is a reason why a person having ordinary skill in the art would have sought to alter Nishizaka's device in a manner inconsistent with its design to function in a manner which undermines its advantages.

3. Conclusion

Accordingly, we reverse the examiner's rejection of Claims 1-3 and 6 under 35 U.S.C. § 103 in view of the combined teachings of Nishizaka, Godejahn and O'Mara.

REVERSED

Teddy S. Gron Administrative Patent Judge	)	
Chung K. Pak Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
Terry J. Owens Administrative Patent Judge	)	

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